

Exhibit 17

JEDEC STANDARD

DDR5 Registering Clock Driver Definition (DDR5RCD01)

JESD82-511

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION



2.1 Pinout

Table 1 specifies the pinout for the DDR5RCD01.

Table 1 — Ball Assignment -240 ball FCBGA, 14 x 19 Grid, TOP VIEW

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NU	QB CA7_A	QB CA3_A	QB CA13_A	QB CA11_A	QB CA12_A	QB CA10_A	QB CA10_B	QB CA12_B	QB CA11_B	QB CA13_B	QB CA3_B	QB CA7_B	NU	A
B	QB CA1_A	V _{SS}	QB CA9_A	V _{SS}	V _{SS}	V _{SS}	V _{DD}	V _{DD}	V _{SS}	V _{SS}	V _{SS}	QB CA9_B	V _{SS}	QB CA1_B	B
C	QB CA6_A	V _{SS}	QB CA8_A	V _{DD}	ZQ CAL	SCL	DERROR _IN_A_n	DERROR _IN_B_n	SDA	V _{DDIO}	V _{DD}	QB CA8_B	V _{SS}	QB CA6_B	C
D	QB CA5_A	V _{SS}	QB CA2_A	V _{DD}	V _{DD}	V _{DD}			V _{DD}	V _{DD}	V _{DD}	QB CA2_B	V _{SS}	QB CA5_B	D
E	QB CA0_A	V _{SS}	QB CA4_A	V _{DD}	QBCK _A_c	QBCK _A_t	V _{SS}	V _{SS}	QBCK _B_t	QBCK _B_c	V _{DD}	QB CA4_B	V _{SS}	QB CA0_B	E
F	QBCS0 _A_n	V _{SS}	QBCS1 _A_n	V _{DD}			V _{DD}	V _{DD}			V _{DD}	QBCS1 _B_n	V _{SS}	QBCS0 _B_n	F
G	QA CA11_A		QA CA13_A	V _{DD}	QDCK _A_c	QDCK _A_t	V _{SS}	V _{SS}	QDCK _B_t	QDCK _B_c	V _{DD}	QA CA13_B		QA CA11_B	G
H	QA CA9_A	V _{SS}	QA CA12_A	V _{DD}	RFU	RFU	V _{DD}	V _{DD}	RFU	RFU	V _{DD}	QA CA12_B	V _{SS}	QA CA9_B	H
J	QA CA10_A	V _{SS}	QA CA3_A	V _{DD}	V _{DD}	V _{DD}	V _{SS}	V _{SS}	V _{DD}	V _{DD}	V _{DD}	QA CA3_B	V _{SS}	QA CA10_B	J
K	QA CA6_A		QA CA7_A	V _{DD}	V _{SS}	V _{SS}	V _{DD}	V _{DD}	V _{SS}	V _{SS}	V _{DD}	QA CA7_B		QA CA6_B	K
L	QA CA1_A		QA CA4_A	V _{DD}	QA CA2_A	QA CA8_A	V _{SS}	V _{SS}	QA CA8_B	QA CA2_B	V _{DD}	QA CA4_B		QA CA1_B	L
M	QA CA5_A	V _{SS}	QA CA0_A	V _{DD}	QACK _A_c	QACK _A_t	V _{DD}	V _{DD}	QACK _B_t	QACK _B_c	V _{DD}	QA CA0_B	V _{SS}	QA CA5_B	M
N	QACS0 _A_n	V _{SS}	QACS1 _A_n	V _{DD}			V _{SS}	V _{SS}			V _{DD}	QACS1 _B_n	V _{SS}	QACS0 _B_n	N
P		V _{SS}			QCCK _A_c	QCCK _A_t	QLBD	QLBS	QCCK _B_t	QCCK _B_c			V _{SS}		P
R	BCS _A_n	BCOM1 _A	BCOM2 _A	BRST _A_n	BCK _A_c	BCK _A_t	V _{SS}	V _{SS}	BCK _B_t	BCK _B_c	BRST _B_n	BCOM2 _B	BCOM1 _B	BCS _B_n	R
T	BCOM0 _A	V _{DD}	V _{DD}	DCS1 _A_n	QRST _A_n		DCK_t	DCK_c		QRST _B_n	DCS0 _B_n	V _{DD}	V _{DD}	BCOM0 _B	T
U	DCA0 _A	V _{SS}	DCS0 _A_n	DLBD_A	DLBS_A	ALERT _n			DRST_n	DLBS_B	DLBD_B	DCS1 _B_n	V _{SS}	DPAR _B	U
V	DCA1 _A	V _{SS}	DCA3 _A	V _{SS}	DPAR _A	V _{SS}	DCA6 _A	V _{SS}	DCA1 _B	V _{SS}	DCA3 _B	V _{SS}	V _{SS}	DCA6 _B	V
W	NU	DCA2 _A	V _{SS}	DCA4 _A	V _{SS}	DCA5 _A	V _{SS}	DCA0 _B	V _{SS}	DCA2 _B	V _{SS}	DCA4 _B	DCA5 _B	NU	W
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Table 2 — Terminal functions

Signal Group	Signal Name	Type	Description
Miscellaneous pins	V _{DD}	Power Input	Power supply voltage
	V _{SS}	Ground Input	Ground
	ZQCAL	Reference	Reference pin for driver calibration
	NU	Mechanical ball	Do not connect on PCB
	RFU[3:0]	I/O	Reserved for future use pins, must be left floating on DIMM and in RCD

1. SA pins are not required for DDR5RCD01 as the address will be hard-coded. Refer to Section 7.5.1, “Target Address,” on page 78 for details.
2. SDA driver operation is dynamic. Depending on the SidebandBus mode of operation (I²C [RW25\[5\]](#) = ‘0’ or I3C Basic [RW25\[5\]](#) = ‘1’), and even on the specific step (byte or bit) of a SidebandBus transaction packet, the SDA output driver can operate either in open-drain mode or push-pull mode.
3. These inputs are 1.0-V inputs.

Naming Convention:

Input Example:

DCAy_N - where ‘y’ is the signal number and ‘N’ is the sub-channel.

Output Example:

QxCAy_N - where ‘y’ is the signal number, ‘x’ is the output copy (A or B) and ‘N’ is the sub-channel.

3 Device Standard

3.1 Description

The DDR5RCD01 is a registering clock driver used on DDR5 RDIMMs and LRDIMMs. Its primary function is to buffer the Command/Address (CA) bus, chip selects, and clock between the host controller and the DRAMs. It also creates a BCOM bus which controls the data buffers for LRDIMMs.

It contains two separate channels which have some common logic such as clocking, but otherwise operate independently of each other. Each channel has a 7-bit double data rate CA bus input, a single parity input, two chip select inputs, and produces two copies of 14-bit single data rate CA bus outputs, and two copies of the chip select outputs. The RCD has a common clock input and PLL, but produces separate clock outputs to the DRAM channels.

10 Electrical - Timing Requirements

10.1 Operating Electrical Characteristics

The DDR5RCD01 parametric values are specified for the device default control word settings, unless otherwise stated.

Table 189 — Operating Electrical Characteristics

Symbol	Parameter	Condition	Min	Nom	Max	Unit
V_{DD}	DC Supply voltage ¹	1.1 V Operation	1.067 (-3%)	1.1	1.166 (+6%)	V
V_{DDIO}	DDR5RCD01 Sideband Interface I/O Supply Voltage		0.95	1.0	1.05	V
T_j	Junction temperature ²		0	-	125	°C
T_{case}	Case temperature	Measurement procedure JESD51-2	-	-	103 ³	°C

1. DC bandwidth limited to 20 MHz.
2. For operation beyond T_j min and max datasheet values are not guaranteed and may de-rate. For operation above T_j max lifetime could be affected. All parametric measurements are performed at 0 °C, 25 °C and 95 °C.
3. This spec is meant to guarantee a T_j of 125 °C by the DDR5RCD01. Since T_j cannot be measured or observed by users, T_{case} is specified instead. Under all thermal condition, the T_j of a DDR5RCD01 shall not be higher than 125 °C.